

REMARKS

Title

Applicants respectfully disagree with the Examiner's assertion that the title of the invention is not descriptive. However, in order to move prosecution of this patent application forward, Applicants have amended the title. Applicants respectfully point out that although the present invention may be used with multiple integrated circuits in a stacked configuration, this is not required.

Drawings

FIG. 23 of the present patent application was inadvertently omitted when the patent application was filed. The omitted, and now proposed new figure, is enclosed herein as FIG. 23. FIG. 23 differs from FIG. 22 only in that conductive interconnects 148 have been placed overlying pads 166 at surface 150 as thoroughly described in the text of the specification at page 10, line 14 through page 11, line 7. Applicants very strongly assert that this new proposed FIG. 23 does not add new matter in any manner. FIG. 22 in combination with the text describing FIG. 23 clearly describe all features of FIG. 23.

Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 6, 7, 11, 14, and 15

Claims 1, 6, 7, 11, 14, and 15 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,333,566 B1 (Nakamura). Claim 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of U.S. Patent 5,291,062 (Higgins).

Applicants respectfully point out that the language of claims 1 and 6 require that the second integrated circuit be outside of the cavity. Claims 1 and 6 expressly state "placing a second integrated circuit adjacent to the first integrated circuit outside the cavity" (emphasis added). Referring to FIG. 7 of Nakamura, Nakamura clearly teaches that the second integrated circuit is inside, not outside, the cavity. Nakamura uses a stage 9 (see FIG. 2(b)) to move the first integrated circuit up in the cavity so that there is room for the second integrated circuit inside the cavity. The present invention does not need the extra process steps required by the use

of stage 9. Thus by placing the second integrated circuit outside of the cavity, the present invention allows use of a different and more efficient process than the one taught by Nakamura.

Claim 2 is allowable for the same reasons as given for claim 1. In addition, Higgins does not teach “electrically connecting the first integrated circuit to the first pads” and “electrically connecting the second integrated circuit to the second pads” where the first pads are on the first surface and the second pads are on the second surface, where the first surface is along a first plane and the second surface is along a second plane, and where the package substrate has a cavity between the first plane and the second plane. Higgins does not teach two integrated circuits having their pads on surfaces in two different planes where there is a cavity between the first and second planes.

The other dependent claims are allowable for at least the same reasons as given for the independent claims.

Claims 3-7 and 9-13

Claims 3-7 and 9-13 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,022,759 (Seki).

Applicants have clarified claim 3 to expressly state “wherein at least one of the first pads is electrically independent of all of the second pads”. Referring to Seki, note that the conducting layer 28 in FIG. 13 was bent upward to form the structure in FIG. 15, and that thus the top surface (30, 31) is still electrically connected to the bottom surface (layer 28). Similarly, each lead part 128 is electrically connected to both the first and second semiconductor elements (151, 152) (see Seki, FIG. 22). Thus there is no argument that Seki teaches “wherein at least one of the first pads is electrically independent of all of the second pads”. Also, Seki teaches that the probe terminals are all on the same surface, namely back surface 134 of the base member 124 (see Seki, FIG. 20 and col. 16, lines 15-24).

Applicants have clarified claim 6 to expressly state “that no substrate is interposed between the first integrated circuit and the second integrated circuit”. Seki clearly teaches that a substrate 124 is interposed between semiconductor elements 151 and 152 (see Seki, FIG. 22). Substrate 124 is a semiconductor base member including base part 126 made of copper (see Seki, col. 15, lines 47-48). Not having an interposing substrate provides at least a cost advantage to the invention of claim 6.

The dependent claims are allowable for at least the same reasons as given for the independent claims.

Claims 3-5

Claims 3-5 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,239,198 (Lin).

Applicants have clarified claim 3 to expressly state that "no substrate is interposed between the first integrated circuit and the second integrated circuit". Lin teaches a substrate 12 interposed between die 20 and die 27 (see Lin, FIG. 4 and col. 3, lines 36-40). Not having an interposing substrate provides at least a cost advantage to the invention of claim 3.

The dependent claims are allowable for at least the same reasons as given for the independent claims.

Claims 6-8

Claims 6-8 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,795,799 (Hosoya).

Applicants have clarified claim 6 to expressly state "that no substrate is interposed between the first integrated circuit and the second integrated circuit". Hosoya, like Lin, teaches a substrate 1' interposed between semiconductor chip 4 and semiconductor chip 4' (see Hosoya, FIG. 3E and col. 4, lines 16-18 and 58-65). Not having an interposing substrate provides at least a cost advantage to the invention of claim 6.

The dependent claims are allowable for at least the same reasons as given for the independent claims.

Claims 3-5, 9, and 10

Claims 3-5, 9, and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya in view Higgins. Claim 9-10 are allowable for the same reasons as given for above for claim 6. Regarding claims 3-5, Higgins does not teach "electrically connecting the first integrated circuit to the first pads" and "electrically connecting the second integrated circuit to the second pads" where the first pads are on the first surface and the second pads are on the

second surface, where the first surface is along a first plane and the second surface is along a second plane, and where the package substrate has a cavity between the first plane and the second plane. Higgins does not teach two integrated circuits having their pads on surfaces in two different planes where there is a cavity between the first and second planes.


Applicant believes the application is in condition for allowance which action is respectfully solicited. Please contact me if there are any issues regarding this communication or the current Application.

Respectfully submitted,

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CLAIMS - VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. A method for forming a package device, comprising:
 - providing a package substrate having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane;
 - attaching a tape to the package substrate along the first plane;
 - placing a first integrated circuit on the tape and in the cavity;
 - depositing encapsulating material over the first integrated circuit;
 - removing the tape;
 - placing a second integrated circuit adjacent to the first integrated circuit outside the cavity; and
 - depositing encapsulating material over the second integrated circuit.
2. The method of claim 1, wherein the package substrate further comprises first pads on the first surface and second pads on the second surface and first bond fingers on the first surface and second bond fingers on the second surface, further comprising;
 - electrically connecting the first integrated circuit to the first pads;
 - electrically connecting the second integrated circuit to the second pads; and
 - testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads.

3(Once Amended). A method of forming a package device, comprising:
providing a package substrate having a first side and a second side and having
first pads on the first side and second pads on the second side;
placing a first integrated circuit on the first side and a second integrated circuit
on a second side, wherein no substrate is interposed between the first
integrated circuit and the second integrated circuit;
electrically connecting the first integrated circuit to the first pads and the
second integrated circuit to the second pads; and
testing the first integrated circuit and the second integrated circuit by applying
test probes to the first pads and the second pads,
wherein at least one of the first pads is electrically independent of all of the
second pads.

4. The method of claim 3, wherein the step of attaching is further characterized by:
the first integrated circuit being placed on the first side prior to the second
integrated circuit being placed on the second side.

5. The method of claim 4, wherein the step of electrically connecting is further
characterized by:
the first integrated circuit being electrically connected to the first pads prior to
the second integrated circuit being electrically connected to the second
pads.

6(Once Amended). A method for forming a package device, comprising:
providing a package substrate having a first surface along a first plane and
second surface along a second plane, wherein the package substrate has a
cavity between the first plane and the second plane;

placing a first integrated circuit in the cavity;
placing a second integrated circuit adjacent to the first integrated circuit
outside the cavity, such that no substrate is interposed between the first
integrated circuit and the second integrated circuit; and
depositing encapsulating material over the first integrated circuit and the
second integrated circuit.

7. The method of claim 6, wherein the step of depositing comprises:
depositing a first portion of the encapsulating material over the first integrated
circuit prior to the step of placing the second integrated circuit; and
depositing a second portion of the encapsulating material over the second
integrated circuit.
8. The method of claim 7, further comprising:
placing a third integrated circuit adjacent to the second integrated circuit prior
to the step of depositing the second portion of encapsulating material.
9. The method of claim 6, wherein the package substrate further comprises first
pads on the first surface, second pads on the second surface, first bond fingers on
the first surface, and second bond fingers on the second surface, further
comprising;
electrically connecting the first integrated circuit to the first pads;
electrically connecting the second integrated circuit to the second pads; and
testing the first integrated circuit and the second integrated circuit by applying
test probes to the first pads and the second pads.

10. The method of claim 9, wherein the step of electrically connecting the first integrated circuit comprises wire bonding.

11. The method of claim 6, wherein the package substrate further comprises a supporting member along the second plane of the substrate.

12. The method of claim 11, wherein the supporting member is between the first integrated circuit and the second integrated circuit.

13. The method of claim 12, wherein the supporting member is electrically conductive.

14. The method of claim 11, further comprising removing the supporting member prior to step of placing the second integrated circuit.

15. The method of claim 14, wherein supporting member is tape.

28(New). The method of claim 7, wherein the step of depositing the first portion of the encapsulating material comprises transfer molding the encapsulating material, and wherein the step of depositing a second portion of the encapsulating material comprises transfer molding the encapsulating material.

29(New). The method of claim 8, wherein the third integrated circuit is stacked at least partially overlying at least one of the first and second integrated circuits.

TITLE - VERSION WITH MARKINGS TO SHOW CHANGES MADE

SEMICONDUCTOR PACKAGE DEVICE FOR USE WITH MULTIPLE
INTEGRATED CIRCUITS IN A STACKED CONFIGURATION AND
METHOD OF FORMATION AND TESTING